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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,445	01/23/2002	David J. Potts	TI-27832	6368

23494 7590 06/15/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,445	POTTS, DAVID J.	
	Examiner	Art Unit	
	Scott B. Geyer	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 25-38* is/are pending in the application.

4a) Of the above claim(s) *31-38* is/are withdrawn from consideration.

5)☒ Claim(s) *12-21 and 25-30* is/are allowed.

6)☒ Claim(s) *1-11,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims 31-38, drawn to an invention non-elected without traverse in the reply filed on 9-22-03. A complete reply to the final rejection must include cancellation of non-elected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-11 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth et al. (5,059,899).

3A. As to ***independent claim 1***, Farnworth et al. teach a method of forming a plurality of integrated circuits on a wafer. Farnworth et al. teach first and second integrated circuit die (30) formed in a first and second positions on a wafer as shown in figure 3, wherein the first and second integrated circuit dies are separated by scribe lines (32). Each integrated circuit die has at least two devices, e.g. a resistor (44) and a transistor (40). The two devices on each integrated circuit die are connected by a metal layers (i.e. control lines) (42). Further, the metal layers (i.e. test circuitry) 46 extend into

the scribe line areas and connect to both the devices on the first and second integrated circuit dies.

3B. As to ***claims 2 and 3***, Farnworth et al. teach physically separating/cutting the two dies (column 3, lines 37-40).

3C. As to ***claims 4 and 5***, Farnworth et al. teach severing the metal layer portion which connects the first and second integrated circuit dies (column 4, lines 25 et seq.).

3D. As to ***claim 6***, Farnworth et al. teach forming a contact (46) in electrical communication with the metal layers (i.e., conductive lines) which connect the first and second integrated circuit dies.

3E. As to ***claim 7***, Farnworth et al. teach testing the at least two integrated circuit dies simultaneously (column 3, lines 1-10).

3F. As to ***claim 8***, Farnworth et al. teach forming an electrical contact (i.e., test circuitry) (46) in the scribe area (32).

3G. As to ***claim 9***, Farnworth et al. teach forming an electrical contact (test bonding pad) 34 in the "first area", i.e. within the area defined by the first integrated circuit.

3H. As to ***claim 10***, Farnworth et al. teach forming an electrical contact in the scribe area (36) for testing both of the integrated circuit dies simultaneously, and forming an electrical contact in both the region of the first IC die and the second IC die. These two electrical contacts are shown in figure 3 by numeral 34. Both of these electrical contacts are communicable with their respective IC circuitry after the dicing step has been performed.

3J. As to ***claim 11***, Farnworth et al. teach the electrical contact (36) in the scribe area as having a larger surface area than the electrical contacts (34) located within the IC die regions.

3K. As to ***claim 22***, Farnworth et al. teach forming a plurality of IC die on the wafer, which comprise a first and second die, as shown by figure 3. Further, Farnworth et al. teach completing circuitry on each of the IC dies and forming a metal layer (i.e., conductive lines) that comprise intra-die portions (i.e., portions within the IC die) and inter-die portions (i.e., portions outside the region defined by the IC die), as is clearly shown by figure 3.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (5,059,899) as applied to claim 1 above, and further in view of Hsu (5,780,161).

5A. As to ***claim 23***, Farnworth et al. teach fabrication of integrated circuits with conductive connectors. Farnworth et al. do not teach formation of the conductive metal connectors using a reticle (i.e., a photomask). However, the use of photomasks is notoriously well known in the art of semiconductor manufacturing. For example, Hsu

teach utilizing a reticle to form the metal patterns on an integrated circuit (column 1, line 14 et seq.). At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the invention of Farnworth et al. by using a photomask (i.e., reticle) as taught for example by Hsu, so as to print fine-line width metal features on a small area surface such as a semiconductor substrate, wherein the use of a reticle would enable more features to be formed on a smaller device area substrate.

Allowable Subject Matter

6. Claims 12-21 and 25-30 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: claims 12, 13, 17 and 29 have been amended by the applicant to independent form incorporating allowable subject matter as detailed in the previous office action. Claims 14-16 are dependent upon claim 13, claims 18-21 are dependent upon claim 17 and 25-28 and 30 are dependent upon claim 29.

Response to Arguments

8. Applicant's arguments filed 5-27-04 have been fully considered but they are not persuasive.

As to the rejection of claims 1-11 and 22, the applicant contends that Farnworth et al. (5,059,899) does not teach the instant invention, since the test circuitry (46) "*does not allow an electrical connection between the two die areas*". However, Farnworth et al. teach "test circuitry 46" as being integrated test circuitry for coordinating the testing

of several dies. To support this, Farnworth et al. has depicted a multitude of lines in figure 3 which connect with the two integrated circuits (30) and with the test circuitry (46), thereby showing that the two integrated circuits are electrically connected. See also column 3, lines 56-68, continuing to column 4, lines 1-38.

The applicant has not introduced any arguments against the rejections of claims 2-11 and 22.

As to the rejection of claim 23, the applicant has stated that whether or not one of ordinary skill in the art would modify Farnworth et al. ('899) "is of no moment" since the resulting construction would not disclose or suggest the invention. The examiner is not quite sure what the applicant means by the phrase "of no moment"...however, it is assumed that the applicant means that the rejection of claim 23 is moot since the applicant believes that independent claim 1 is allowable. However, the instant office action rejects independent claim 1 under Farnworth et al. ('899) and 23 also still stands as rejected under Farnworth et al. ('899) in view of Hsu ('161), as detailed above.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (571) 272-1958. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is

703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SBG
June 10, 2004

Primary Examiner
AU 2827